

CLAIMS

We claim:

1. A method for assembling a semiconductor chip package, the method comprising:

5 providing a substrate having a metallization layer formed on a single side of the substrate;

attaching a semiconductor die to the substrate;

10 electrically connecting the semiconductor die to a portion of the metallization layer;

15 mounting an electromagnetic interference shield on the substrate; and

encapsulating at least a portion of the shield and the semiconductor die with a mold material.

2. The method of claim 1, wherein mounting the shield on the substrate

15 comprises electrically connecting the shield to a portion of the metallization layer.

3. The method of claim 1, wherein providing the substrate having the metallization layer formed on a single side of the substrate comprises providing within the metallization layer a die pad, a plurality of bond pads and a plurality of solder pads.

20

4. The method of claim 3, wherein electrically connecting the semiconductor die to a portion of the metallization layer comprises forming a bond wire between the semiconductor die and one of the bond pads.

5. The method of claim 1, wherein mounting the shield on the substrate comprises attaching the shield to the substrate with epoxy.

6. The method of claim 1, wherein mounting the shield on the substrate  
5 comprises attaching the shield to the substrate with solder.

7. The method of claim 3, wherein mounting the shield on the substrate comprises matching a plurality of recesses on a corresponding plurality of legs of the shield with a corresponding plurality of the bond pads.

10

8. The method of claim 3, wherein mounting the shield on the substrate comprises attaching the legs of the shield to the corresponding plurality of the bond pads with solder.

15

9. The method of claim 3, wherein mounting the shield on the substrate comprises matching a plurality of projections on a corresponding plurality of legs of the shield with a corresponding plurality of recesses on a corresponding plurality of the bond pads.

20

10. The method of claim 1, further comprising providing the shield with a plurality of rounded corners.

11. A semiconductor chip package comprising:  
25 a substrate;  
a metallization layer formed on one side of the substrate;

a semiconductor die mounted on the substrate, the semiconductor die being electrically connected to a portion of the metallization layer;

a shield element mounted on the substrate, the shield element being electrically connected to a portion of the metallization layer; and

5 a package mold surrounding the semiconductor die and the shield element.

12. The semiconductor chip package of claim 11, wherein the metallization layer comprises:

a die pad formed on the substrate; and

10 a plurality of bond fingers formed on the substrate;

wherein the semiconductor die is attached to the die pad; and

wherein the shield element is attached to at least one of the bond fingers.

13. The semiconductor chip package of claim 12, further comprising a bond  
15 wire forming an electrical connection between a bond pad on the semiconductor die and  
one of the bond fingers.

14. The semiconductor chip package of claim 11 wherein the shield element  
comprises:

20 a substantially planar top surface; and

a plurality of substantially planar side surfaces, the side surfaces being joined to  
the top surface and to each other with rounded corners.

15. The semiconductor chip package of claim 11 wherein the shield element  
25 comprises:

a horizontal top surface; and  
at least one vertical side surface, the side surface being joined to the top surface  
with a rounded corner.

5        16. The semiconductor chip package of claim 15 wherein the shield element  
comprises a plurality of openings formed in the top and side surfaces.

17. The semiconductor chip package of claim 15 wherein the top surface of  
the shield element is circular in shape.

10        18. The semiconductor chip package of claim 12 wherein the shield element  
comprises a plurality of legs attached to a corresponding plurality of the bond fingers.

15        19. The semiconductor chip package of claim 12 wherein at least one the  
legs of the shield element comprises a concave lower surface shaped to receive a  
corresponding one of the bond fingers.

20        20. The semiconductor chip package of claim 12 wherein at least one the  
legs of the shield element comprises a convex lower surface, and wherein a  
corresponding one of the bond fingers comprises a concave upper surface shaped to  
receive the convex lower surface of the leg.

21. A shielded semiconductor device package comprising:  
a substrate having a metallization pattern formed on one side of the substrate,  
25 the metallization pattern having a plurality of solderable surface mount pads;

a semiconductor device electrically attached to the metallization pattern and mechanically attached to the substrate;

a metal screen enclosing the semiconductor device and electrically and mechanically attached to a portion of the metallization pattern to shield the

5 semiconductor device from radio frequency energy; and

an insulating material transfer molded about the semiconductor device and encapsulating the metal screen.

Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20